

FIG.1

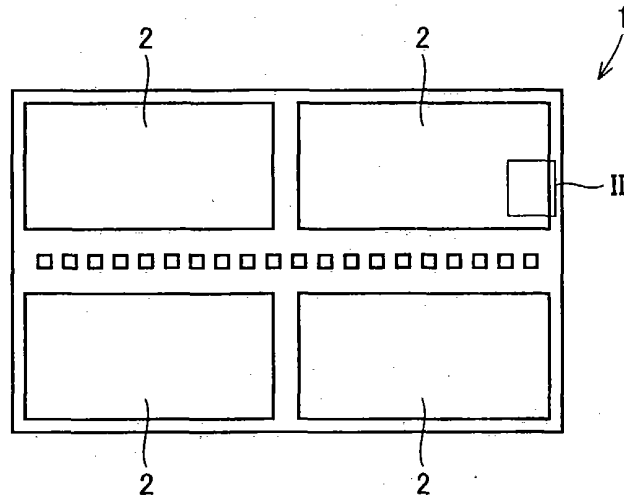


FIG.2

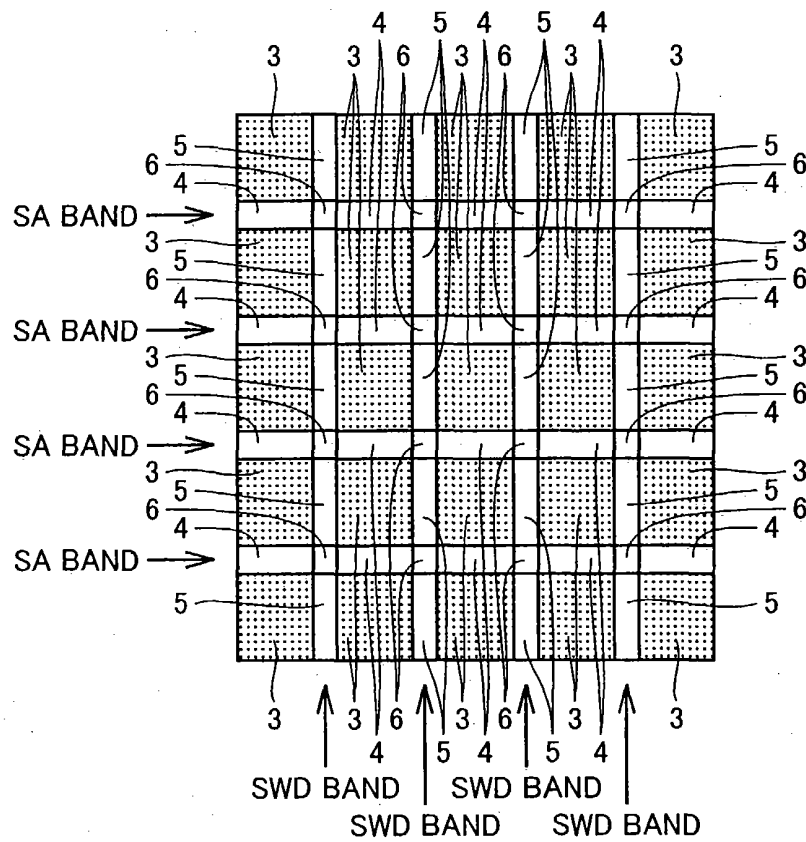


FIG.3

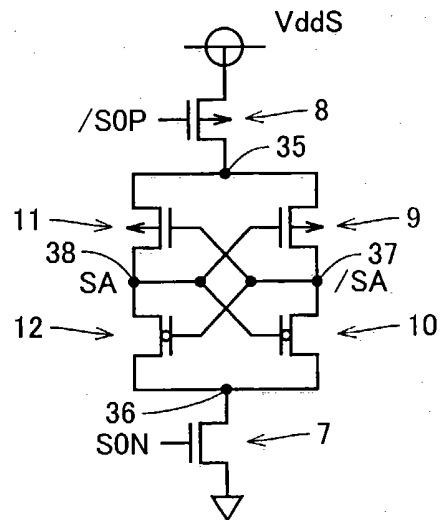


FIG.4

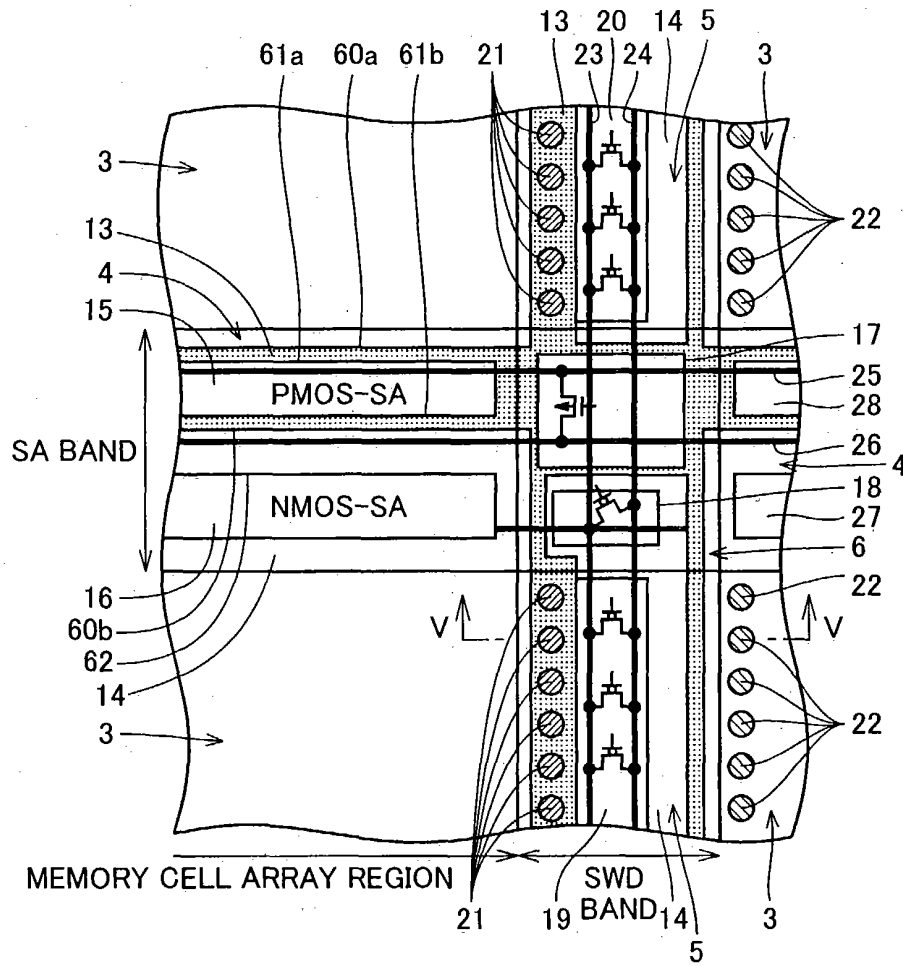


FIG.5

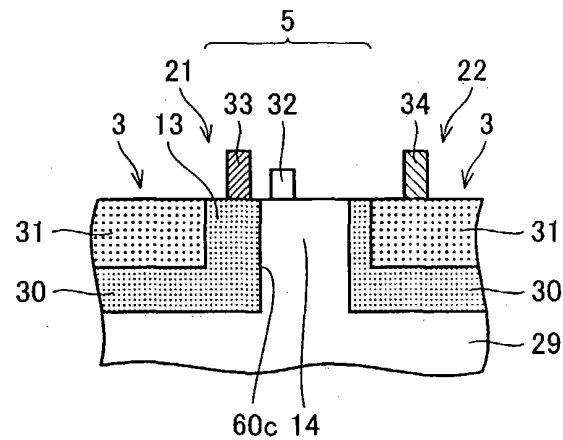


FIG.6

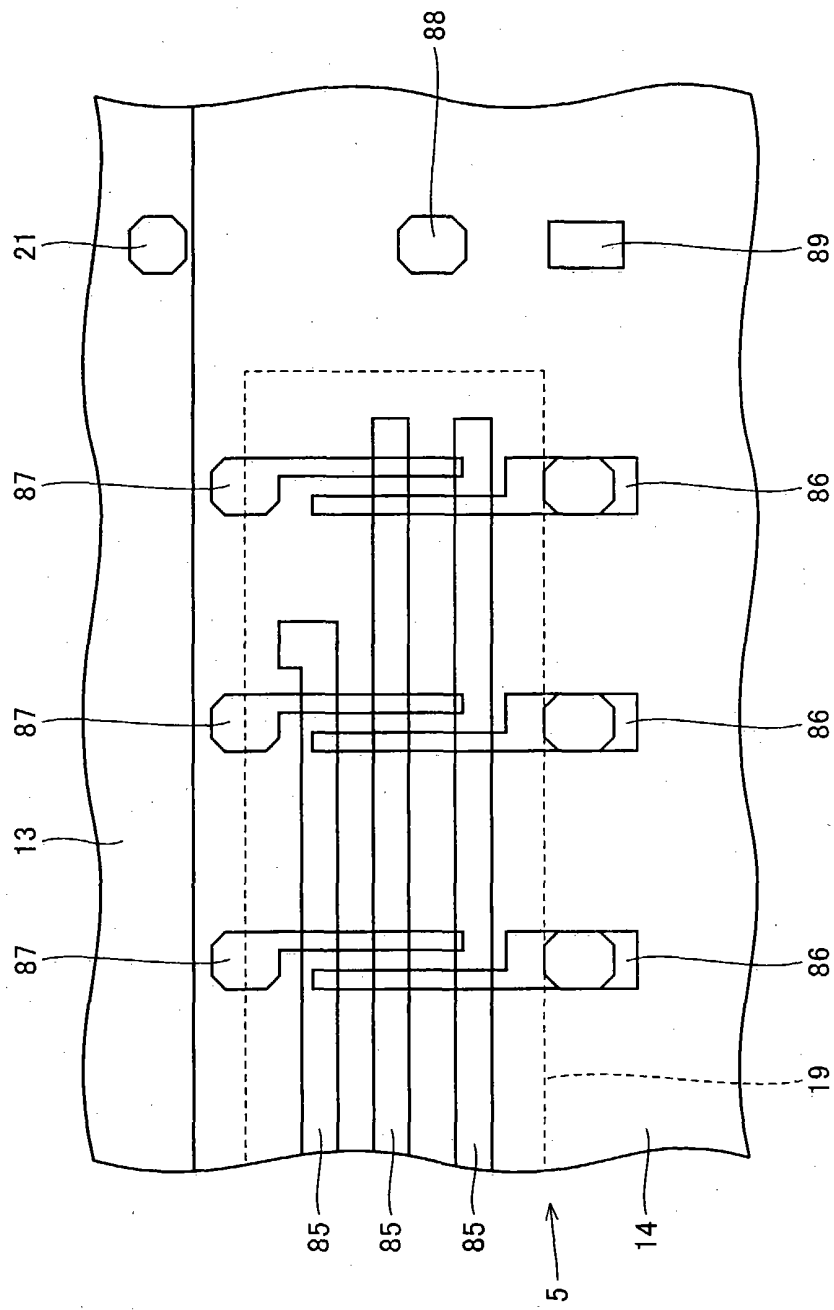


FIG.7

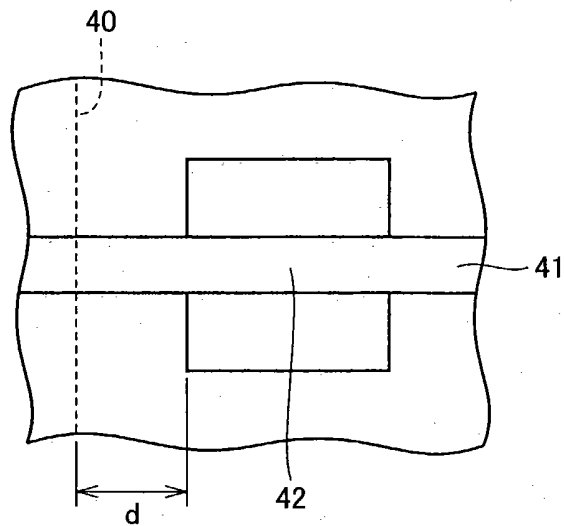


FIG.8

VARIATION AMOUNT  
OF  $V_{th}$  :  $\Delta V_{th}$   
(mV)

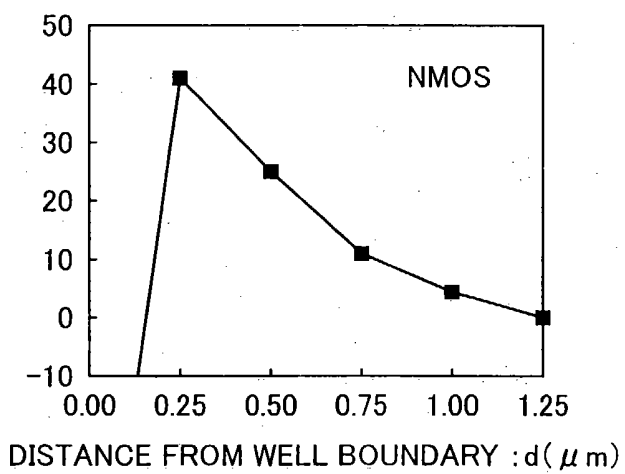


FIG.9

VARIATION AMOUNT  
OF  $V_{th}$  :  $\Delta V_{th}$   
(mV)

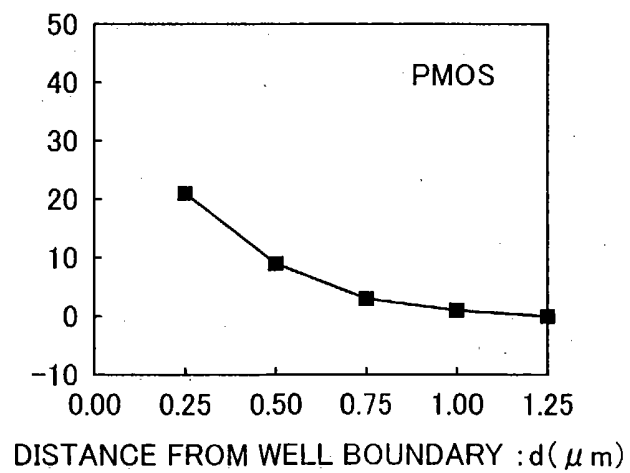


FIG.10

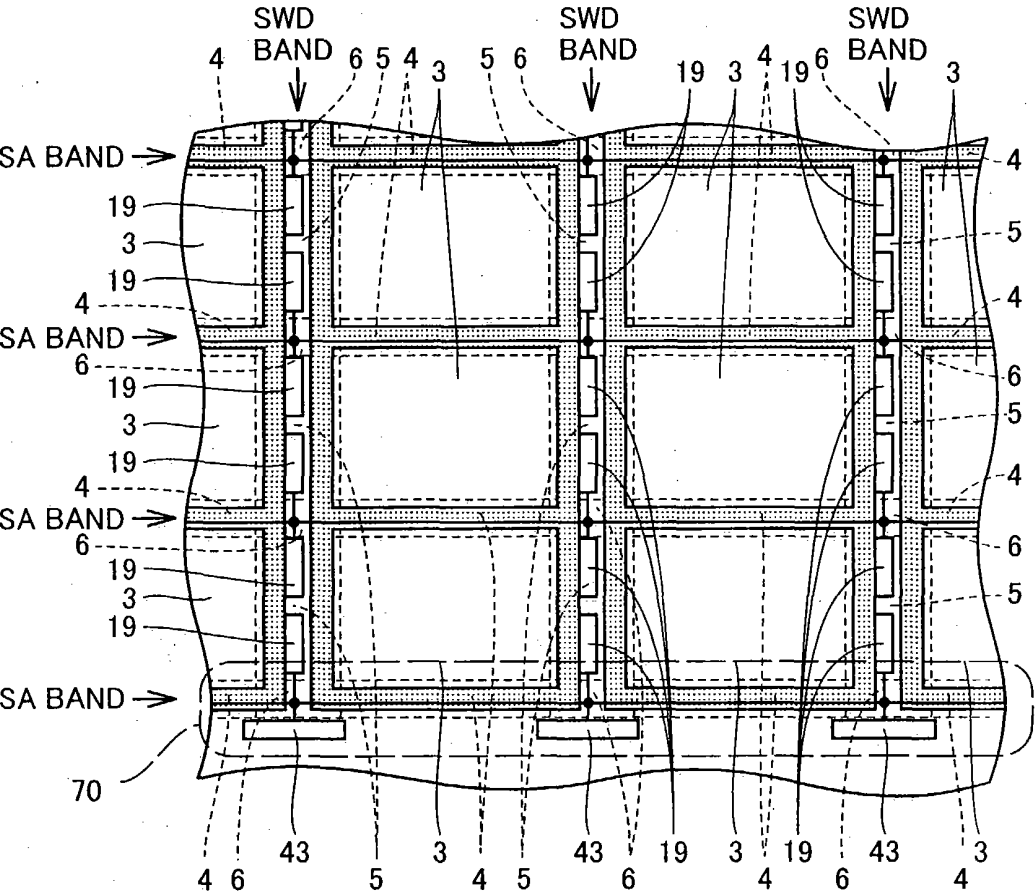


FIG.11

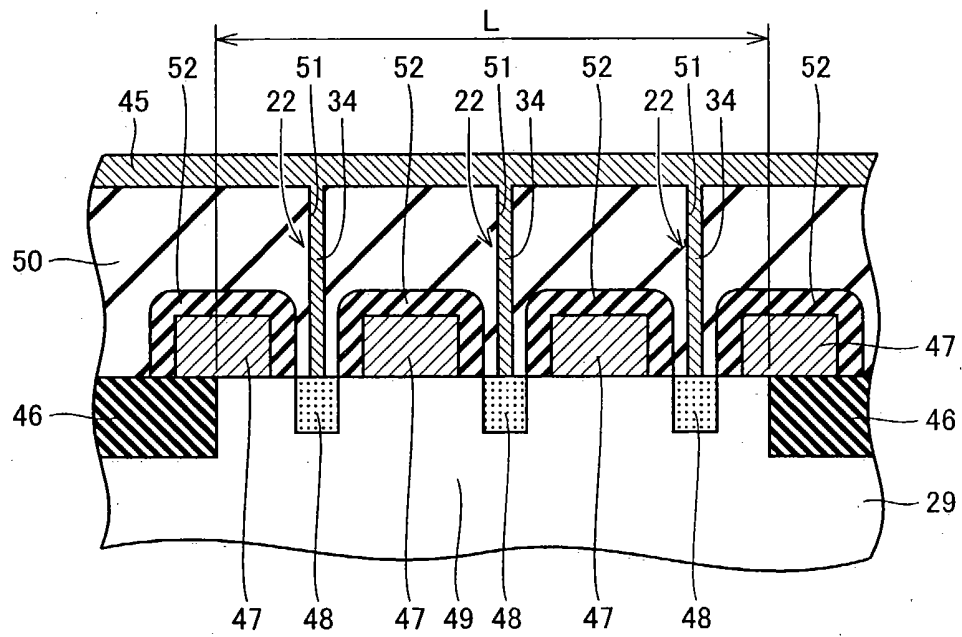
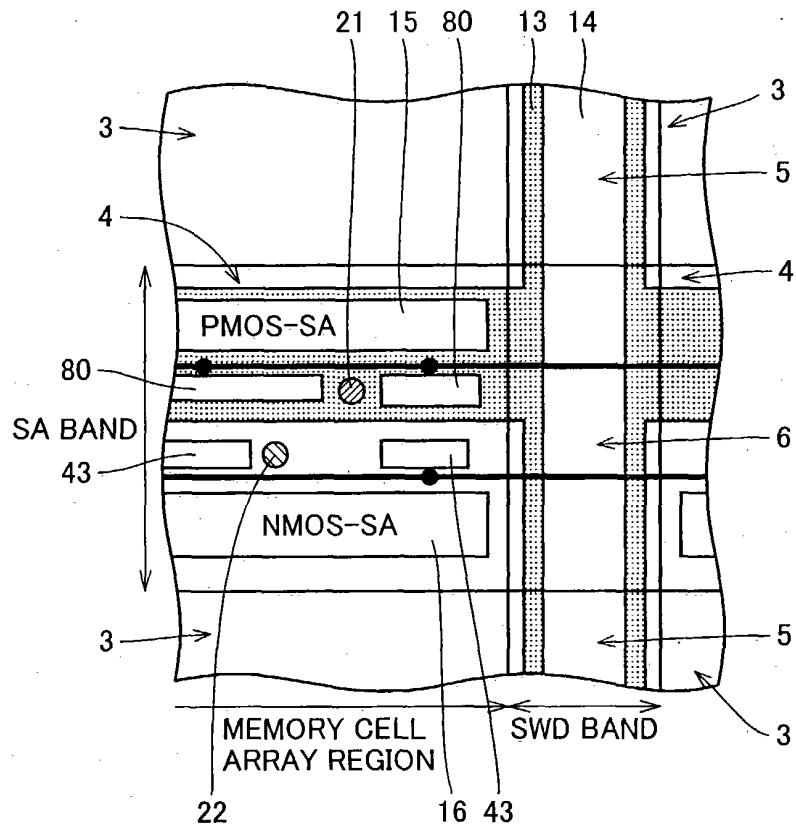


FIG.12





This diagram shows a cross-sectional view of a semiconductor device. It features a central region labeled "MEMORY CELL ARRAY REGION" and a vertical strip on the right labeled "SWD BAND". The device includes a "PMOS-SA" (P-type Source Access) region and an "NMOS-SA" (N-type Source Access) region. A "SA BAND" (Source Access Band) is indicated on the left, containing several circular features. The device is divided into regions by vertical lines, with labels 21, 15, 22, 13, 17, and 14 indicating specific vertical boundaries or layers. Other labels include 3, 4, 5, 6, 81, and 9, which likely refer to different layers or components of the device structure.

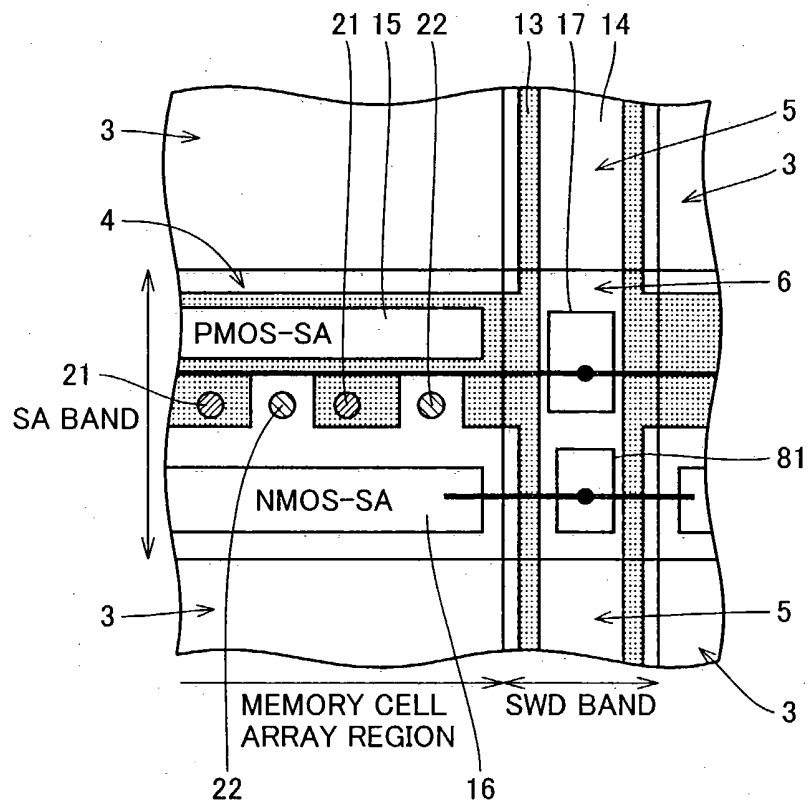


FIG.14

